WHAT IS CLAIMED IS:

Sub B3

1. A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising at least one register file with a plurality of registers, said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a load instruction to retrieve at least one data word from said memory and parse said at least one data word over selected parts of at least two data registers in said at least one register file, wherein the number of said at least two data registers is greater than the number of said at least one data word.

2. The data processing system of claim 1 wherein said load instruction selects sign or zero extend for the parsed data in said at least two data registers.

3. The data processing system of claim 1 wherein said parse comprises unpacking the lower and higher half-words of each at least one data word into a pair of data registers.

4. The data processing system of claim 3 wherein said at least one data word is two data words, and said parse comprises unpacking the lower and higher half-words of each of said two data words into corresponding pairs of data registers.

5. The data processing system of claim 4 wherein said unpacking of said lower and higher half-words of said data words is interleaved.

6. The data processing system of claim 5 wherein said at least one register file is two register files, and one pair of said corresponding pairs of data registers is located in one register file and the other pair is located in the other register file.

7. The data processing system of claim 1 wherein said parse comprises unpacking the bytes of each at least one data word into the lower and higher half-words of each of a pair of data registers.

8. The data processing system of claim 7 wherein said at least one data word is two data words, and said parse comprises unpacking eight bytes from said two data words into corresponding pairs of data registers.

9. The data processing system of claim 8 wherein said unpacking of said bytes of said data words is interleaved.

10. The data processing system of claim 9 wherein said at least one register file is two register files, and one pair of said corresponding pairs of data registers is located in one register file and the other pair is located in the other register file.

11. The data processing system of claim 7 wherein said at least one register file is two register files, and said

pair of data registers are an even/odd pair in the same data register file.

12. The data processing system of claim 7 wherein said at least one register file is two register files, one of said pair of data registers is located in one register file and the other is located in the other register file, and each of said pair of data registers has the same relative register number.

13. A data processing system comprising:

a memory comprising a plurality of memory locations; and

a central processing unit core comprising at least one register file with a plurality of registers, said core connected to said memory for loading data from and storing data to said memory locations, said core responsive to a store instruction to concatenate data from selected parts of at least two data registers into at least one data word and save said at least one data word to said memory, wherein the number of said at least two data registers is greater than the number of said at least one data word.

14. The data processing system of claim 13 wherein said at least two data registers are two data registers and said concatenate comprises packing the lower half-words of said two data registers into the lower and higher half-words of said at least one data word.

15. The data processing system of claim 14 wherein said two data registers are an even/odd register pair.

16. The data processing system of claim 14 wherein said at least one register file is two register files, one of said two data registers is located in one register file and the other is located in the other register file, and each of said two data registers has the same relative register number.

17. The data processing system of claim 13 wherein said at least two data registers are four data registers, said at least one data word is two data words, and said concatenate comprises packing the lower half-words of said four data registers into the lower and higher half-words of each of said two data words.

18. The data processing system of claim 17 wherein said at least one register file is two register files, and said four data registers are even/odd register pairs in each register file with the same relative starting register number.

19. The data processing system of claim 13 wherein said at least two data registers are two data registers, and said concatenate packs the lower bytes of the lower and higher half-words of each of said two data registers into said at least one data word.

20. The data processing system of claim 13 wherein said at least two data registers are four data registers, said at least one data word is two data words, and said concatenate packs the lower bytes of the lower and higher half-words of each of said four data registers into said two data words.